CLAIM AMENDMENTS

The claims have been amended as follows:

2. (Amended) The processing circuit [unit] of claim 1, wherein the chain of processing units comprises a systolic chain.

5. (Amended) The processing circuit of claim 4, wherein each processing unit [circuit] comprises a first input terminal to receive the indications of the discrete input values from a processing unit [circuit] input line common to the processing units [circuits] and a second input terminal to receive the indications of the discrete input values from another processing unit [circuit], the multiplexer coupling the first and second terminals of one of the processing units [circuits] together to designate the point in the chain at which the accumulation begins.

6. (Amended) The processing circuit of claim 1, wherein each processing unit [circuit] comprises:

a first adder circuit to generate an indication of a summation of two of the discrete input values; and

a multiplier circuit coupled to the first adder circuit to generate an indication of a product of a coefficient associated with said each processing unit [circuit] and the summation of the two discrete values.

7. (Amended) The processing circuit of claim 6, further comprising:

a second adder circuit coupled to the first multiplier circuit to combine the summation of the two discrete input values with a progressive summation provided by another processing unit [circuit].

11. (Amended) The processing circuit of claim 1, wherein the processing units and tap selection circuit comprise at least part of [circuit comprises] a finite impulse response filter.